CLAIMS:

1. A signal processing apparatus (158c) for use in a high speed digital communication system (10), said signal processing apparatus (158c) performing predefined signal processing functions, comprising:

an input receiving input digital information,

an array-type processor (120) configured to execute signal processing function code using said input digital information, said function code corresponding to at least one of said predefined signal processing functions responsivag to a current system state;

at least one system controller (170) configured to: detect a change of said system state in said high speed digital communication system (10); and dynamically reconfigure said array-type processor (10), in real-time or in near real-time, to execute signal processing function code corresponding to at least one of said signal processing functions responsivag to said detected change of system state.

2. The signal processing apparatus (158c) of Claim 1, wherein said array-type processor (120) is comprised of a plurality of data processors (122), wherein each of said data processors (122) in said array-type processor includes a dedicated program memory (124) configured to store said signal processing function code, and wherein said plurality of data processors (122) are operativag to execute said signal processing function code stored in the respectivag dedicated program memories (124).

3. The signal processing apparatus (158c) of Claim 2, wherein the act of dynamically reconfiguring said array-type processor (120) comprises the acts of:

downloading from an external memory (130), said signal processing function code corresponding to said at least one of said signal processing functions responsivag to saidletected change of system state;

storing at least a portion of said downloaded signal processing function code the dedicated program memories (124) of one or more of said plurality of data processors (120); and

executing said downloaded signal processing function code in said one or more of said plurality of data processors (120).

4. The signal processing apparatus (158c) of Claim 1, further comprising an input data interface (110) configured to buffer said input digital input information, said input data interface (110) having an output coupled to an input of said array-type processor (120).

5. The signal processing apparatus (158c) of Claim 1, further comprising an output data interface (160) configured to buffer digital output information output from said array-type processor, said output data interface having an input coupled to an output of said array-type processor.

6. The signal processing apparatus (158c) of Claim 2, wherein said dedicated memory (124) is configured as a plurality of switch selectable memory banks (125a-n).

7. The signal processing apparatus (158c) of Claim 2, wherein the at least one system controller is configured to switchably select one of the plurality of memory banks 125a-n) responsivag to said detected change of system state.

8. The signal processing apparatus (158c) of Claim 6, wherein each of said plurality of memory banks (125a-n) is configured to store signal processing function code associated with one of said predetermined signal processing functions.

9. A method for reconfiguring a signal processing device (158c) to perform signal processing functions in real time or in near real time, said method, for use in a network node of a high speed digital communication system, comprising the acts of:

receiving input digital information at said network node;

detecting a change of state in said network node;

identifying at least one signal processing function to be executed responsivag to said detected change of state in said network node; and

dynamically reconfiguring, in real time or in near real-time, the signal processing device (158c) to execute said at least one signal processing function, responsivag to said detected change of system state.

10. The method of Claim 9, wherein the act of detecting a change of state in said network node is made in accordance with one or more criteria including: (i) channel and system data (ii) protocols defined by a prevailing network standard under which the network node is operating, (iii) said received input digital information, and (iv) output data associated with the signal processing device.

11. The method of Claim 10, wherein the act of re-configuring the signal processing device further comprises the acts of:

retrieving, from an external memory (130), predetermined signal processing function code data responsivag to said detected change of system state; and

storing said retrieved signal processing function code data in an array-type processor (120) of said signal processing device (158c).

12. The method of Claim 11, wherein said array-type processor is comprised of an array (120) of data processors (122), each data processor (122) in said array (120) including a dedicated memory (124) configured to store signal processing function code data.